REMARKS

Applicant thanks the Examiner for the very thorough consideration given the present application.

Claims 1-6 are now present in this application. Claims 1, 2, 3 and 6 are independent.

Claims 1 and 6 have been amended. Reconsideration of this application, as amended, is respectfully requested.

Drawings

Applicant has not received a Notice of Draftsperson's Patent Drawing Review PTO-948 indicating whether or not the formal drawings have been approved by the Draftsperson. Clarification in the next Office Action is respectfully requested.

Rejections under 35 U.S.C. § 102

Claims 1 and 6 stand rejected under 35 U.S.C. § 102(a) as being anticipated by U.S. Patent No. 5,157,573 to Lee et al. (Lee) for the reasons set forth in paragraph 2 of the Office Action. This rejection is respectfully traversed.

Lee discloses a pad 10, which is connected to resistors 22 via a direct short created by line 21 (see Lee, Fig.3). Lee also discloses logic devices

connected to line 18. However, the logic devices (asserted by the Examiner to be chips) and the pad 10 are not directly shorted through line 21, and neither are they directly shorted through line 18. This is because p channel field effect transistor (FET) 14 intervenes between the two, making a direct short connection between the pad and the logic devices impossible. The rejection under 35 U.S.C. 102 is not proper.

Particularly, Lee fails to teach a pad, a main chip, and a conductor, said conductor creating a direct short connection between said pad and main chip, as recited in independent claim 1, as amended, and similarly stated in independent claim 6, as amended. Reconsideration and withdrawal of this art grounds of rejection are respectfully requested.

Conclusion

All of the stated grounds of rejection have been properly traversed, accommodated, or rendered moot. Applicant therefore respectfully requests that the Examiner reconsider all presently outstanding rejections and that they be withdrawn. It is believed that a full and complete response has been made to the outstanding Office Action, and as such, the present application is in condition for allowance.

If the Examiner believes, for any reason, that personal communication will expedite prosecution of this application, the Examiner is invited to telephone Percy L. Square, Registration No. 51,084 at (703) 205-8034, in the Washington, D.C. area.

Prompt and favorable consideration of this Amendment is respectfully requested.

Attached hereto is a marked-up version of the changes made to the application by this Amendment.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment or credit any overpayment to Deposit Account No. 02-2448 for any additional fees required under 37 C.F.R. §§ 1.16 or 1.17; particularly, extension of time fees.

Respectfully submitted,

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Attachment: Version with Markings to Show Changes Made

VERSION WITH MARKINGS TO SHOW CHANGES MADE

In the Claims:

The claims have been amended as follows:

1. (Three Times Amended) An ESD (Electro-Static-Discharge) protection circuit comprising:

a pad, [and] a main chip, and a conductor, said conductor creating a direct short connection between said pad and main chip; and,

a plurality of transistors, each connected between the pad and the main chip, said transistors having a plurality of resistors connected to an input terminal, said resistors being connected in parallel with each other, and having no resistor connected between said transistors and ground, to discharge static electricity through said transistors to ground and avoid reduction in gain.

6. (Twice Amended) An ESC (Electro-Static-Discharge) protection circuit comprising:

a pad, [and] a main chip, and a connector, said connector directly shorting said paid and main chip; and

a plurality of transistors, each connected between the pad and the main chip, having resistors connected to an input terminal only, to discharge static electricity through said transistors to ground and avoid reduction in gain.